IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS

In re Patent Application of: **CROCE ET AL.**	
Serial No. **09/839,596**	Examiner: **ORI NADAV**
Filed: **APRIL 20, 2001**	Art Unit: **2811**
For: **RESURF LDMOS INTEGRATED STRUCTURE**	Attorney Docket No. **53288**

APPELLANTS' APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is Appellants' Appeal Brief (in triplicate) together with the requisite $330.00 fee for filing a brief. If any additional extension and/or fee is required, authorization is given to charge Deposit Account No. **01-0484**.

(1) REAL PARTY IN INTEREST

The real party in interest for the present application is the assignee, STMicroelectronics S.r.l.

(2) RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences for the present application.

(3) STATUS OF CLAIMS

Claims 5-25 are pending in the present application with Claims 19-25 withdrawn from consideration. Claims 5-18 are all rejected. Accordingly, Claims 5-18 are the subject of this appeal.

(4) **STATUS OF AMENDMENTS**

No Amendments were filed after final. Accordingly, the claims in the Appendix incorporate all prior amendments.

(5) **CONCISE SUMMARY OF THE INVENTION**

As described on page 5, lines 3-23 of the present specification, while referring to FIGs. 2b and 3b, for example, the present invention is directed to a lateral diffused metal oxide semiconductor (LDMOS) integrated device. The present invention provides a relatively simple and effective approach to address punch-through (PT) problems that normally limit the performance of known RESURF LDMOS structures when operating as high side drivers. The LDMOS structure of the invention includes a superficial or surface portion (or body buffer region) 15 of the drain well region 12 which surrounds the body region 13. The body buffer region 15 is preferably more heavily doped than the remaining portion of the drain well region 12, as shown in FIG. 2b (FIGs. 2a and 2b reproduced below).

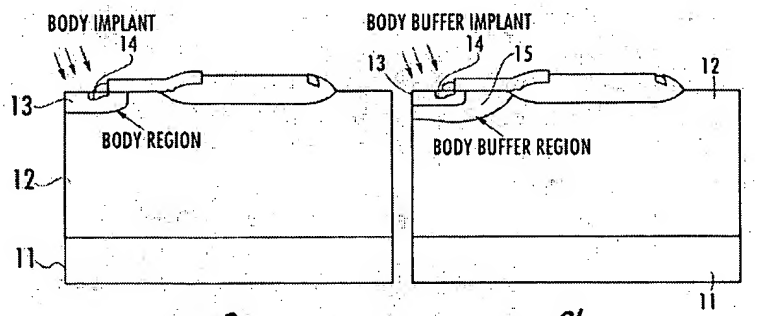


FIG. 2a. (PRIOR ART)

FIG. 2b.

By making the body buffer region 15 more heavily doped than the remainder of the drain well region 12, a

significant enhancement of the RESURF LDMOS structure performance is achieved, especially when functioning as a high side driver at relatively high VDS voltages. As opposed to what occurs in the remainder of the drain well region 12, the body buffer region 15 is not completely depleted during operation. Thus, punch-through problems that restrict the conditions under which present LDMOS structures may safely be used are reduced.

As shown in FIG. 3b (reproduced below), even if relatively high voltages are applied to the drain and source (typical of a high-side application), the drain well region 12 will be completely depleted of its charge before the body buffer region 15 is depleted. This is due to the heavier doping of the body buffer region 15. This substantially prevents the occurrence of PT phenomena at relatively low voltages, which in turn enhances the performance of the structure of the invention under critical conditions of use.

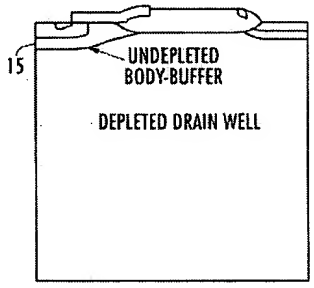


FIG. 3b.

(6) **ISSUES**

The issues presented on appeal are: whether Claim 5 is patentable under 35 U.S.C. §102(b) as being anticipated by Huang (U.S. 5,665,988); and whether Claims 6-18 are patentable

under 35 U.S.C. §103(a) over Huang alone or in combination with Contiero et al. (U.S. 5,041,895).

(7) GROUPING OF CLAIMS

For the purposes of addressing the rejections under 35 U.S.C. §102(b) and 35 U.S.C. §103(a), the grouping of the claims is: Claims 5-18 stand together as a group.

(8) ARGUMENT

Claims 5-18 were rejected in view of Huang (U.S. 5,665,988) taken alone or in combination with Contiero et al. (U.S. 5,041,895) for the reasons set forth on pages 2-5 of the Final Office Action. Appellants contend that Claims 5-18 clearly define over the cited references, and in view of the following remarks, reversal of the rejections under 35 U.S.C. §102(b) and §103(a) is requested.

As recited in independent Claim 5, for example, the LDMOS device includes a semiconductor substrate and a drain region of a first conductivity type adjacent the semiconductor substrate and including a superficial buffer region being more heavily doped than adjacent portions of the drain region. Moreover, the LDMOS device also includes a body region completely surrounded on a bottom and sides thereof by the buffer region and having a second conductivity type, and a source region in the body region and having the first conductivity type. The LDMOS device thus provides a RESURF structure that may be used at relatively high voltages yet with a reduction in punch through problems, as discussed above.

Independent Claim 14 is directed to a related LDMOS

integrated device. This claim also recites that the body region is completely surrounded on a bottom and sides thereof by the buffer region as in Claim 5.

The Examiner has relied on the Huang patent as allegedly teaching the use of an LDMOS integrated device as claimed (page 2 of the Final Office Action). However, the Examiner is wrong. No device in the Huang patent is or can be characterized as an LDMOS device, as incidentally acknowledged by the Examiner in his remarks on page 4 of the Office Action. More accurately (referring to FIG. 1 of Huang reproduced below), Huang is directed to an insulated gate bipolar transistor (IGBT) including a buffer region **13** completely surrounding a p-type minority carrier injection region **9** (referred to by the Examiner as the claimed body region). The Examiner also refers to "a drain region **2**" comprising the buffer region **13** in Huang.

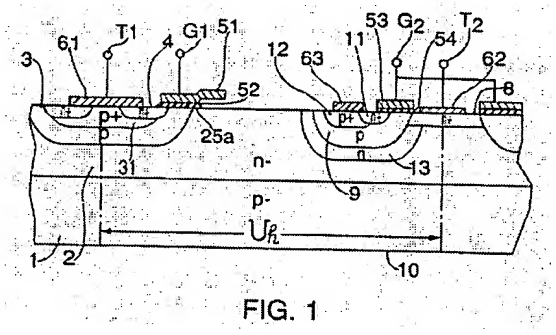


FIG. 1

Appellants maintain that the Examiner has mischaracterized the cited reference. Indeed, referring to Fig. 1 and the associated description in columns 6 and 7 of Huang, layer **2** is more accurately a high resistance surface layer of the substrate **1**. The actual drain region **8** of the

lateral IGBT does not include the buffer region **13**.

Furthermore, as should be clear to the Board and the Examiner, the structures of Huang are not LDMOS structures at all. Indeed, the p-type base region **3**, which is the body of the intrinsic MOS transistor, is not surrounded by the buffer region **13**. The p-type region **3** is underneath the gate electrode **51** in which an inversion layer is induced (see Col. 7, lines 17-21 of Huang). As is appreciated by those skilled in the art, this is the common definition of the body of a MOS transistor.

As the Examiner and Board are aware, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim.

The cited reference to Contiero et al. was relied upon by the Examiner for teaching the use of various dopants for certain regions of an integrated structure. It is sufficient to note that the Contiero et al. patent does not disclose an LDMOS device as claimed, and does not make up for any of the deficiencies of Huang noted above.

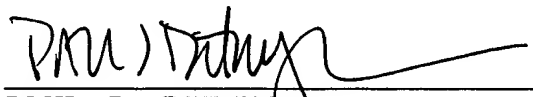
There is simply no teaching or suggestion in the cited references to provide the combination of features as claimed. Accordingly, for at least the reasons given above, Appellants maintain that the cited references do not disclose or fairly suggest the invention as set forth in Claims 5 and 14. Furthermore, no proper modification of the teachings of these references could result in the invention as claimed. Thus, the rejections under 35 U.S.C. §102(b) and §103(a) should be reversed.

It is submitted that the independent claims are patentable over the prior art. In view of the patentability of the independent claims, it is submitted that their dependent claims, which recite yet further distinguishing features are also patentable over the cited references for at least the reasons set forth above. Accordingly, these dependent claims require no further discussion herein.

CONCLUSIONS

In view of the substantive arguments presented above, it is submitted that all of the claims, namely Claims 5-18, are patentable over the prior art. Accordingly, Appellants respectfully request that all of the rejections be reversed.

Respectfully submitted,



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APPENDIX INCLUDING THE CLAIMS ON APPEAL

FOR U.S. PATENT APPLICATION SERIAL NO. 09/839,596

5. (Previously presented) A lateral diffused metal oxide semiconductor (LDMOS) integrated device comprising:

a semiconductor substrate;

a drain region of a first conductivity type adjacent said semiconductor substrate and comprising a superficial buffer region being more heavily doped than adjacent portions of said drain region;

a body region completely surrounded on a bottom and sides thereof by said buffer region and having a second conductivity type; and

a source region in said body region and having the first conductivity type.

6. (Previously presented) The LDMOS integrated device of Claim 5 wherein said drain region has a depth of about 1.5 to 4.5 micrometers.

7. (Previously presented) The LDMOS integrated device of Claim 5 wherein the portions of said drain region adjacent said superficial buffer region have a dopant concentration of about $2.5x10^{15}$ to $2.5x10^{16}$ atoms cm^{-3}.

8. (Previously presented) The LDMOS integrated device of Claim 5 wherein said superficial buffer region has a depth of about 0.15 to 0.45 micrometers.

9. (Previously presented) The LDMOS integrated

device of Claim 5 wherein said superficial buffer region has a dopant concentration of about $5x10^{16}$ to $5x10^{17}$ atoms cm^{-3}.

10. (Previously presented) The LDMOS integrated device of Claim 5 wherein said body region has a depth of about 0.25 to 0.75 micrometers.

11. (Previously presented) The LDMOS integrated device of Claim 5 wherein said body region has a dopant concentration of about $5x10^{17}$ to $5x10^{18}$ atoms cm^{-3}.

12. (Previously presented) The LDMOS integrated device of Claim 5 wherein said drain region is doped with phosphorous; and wherein said body region is doped with boron.

13. (Previously presented) The LDMOS integrated device of Claim 5 wherein said drain region is doped with boron; and wherein said body region is doped with phosphorus.

14. (Previously presented) A lateral diffused metal oxide semiconductor (LDMOS) integrated device comprising:

a semiconductor substrate;

a drain region of a first conductivity type adjacent said semiconductor substrate and comprising a superficial buffer region being more heavily doped than adjacent portions of said drain region;

said superficial buffer region having a dopant concentration of about $5x10^{16}$ to $5x10^{17}$ atoms cm^{-3} and the adjacent portions of said drain region having a dopant concentration of about $2.5x10^{15}$ to $2.5x10^{16}$ atoms cm^{-3};

a body region completely surrounded on a bottom and sides thereof by said superficial buffer region and having a second conductivity type; and

a source region in said body region and having the first conductivity type.

15. (Previously presented) The LDMOS integrated device of Claim 14 wherein said drain region has a depth of about 1.5 to 4.5 micrometers.

16. (Previously presented) The LDMOS integrated device of Claim 14 wherein said buffer region has a depth of about 0.15 to 0.45 micrometers.

17. (Previously presented) The LDMOS integrated device of Claim 14 wherein said body region has a depth of about 0.25 to 0.75 micrometers.

18. (Previously presented) The LDMOS integrated device of Claim 14 wherein said body region has a dopant concentration of about $5x10^{17}$ to $5x10^{18}$ atoms cm^{-3}.

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 10th day of June, 2004.